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SIMULATION OF VLSI DESIGN FOR CONVOLUTIVE BLIND SOURCE SEPARATION

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ABSTRACT

This brief presents an efficient very-large-scale integration architecture design for convolutive blind source separation (CBSS). The CBSS separation network derived from the information maximization (Infomax) approach is adopted. The proposed CBSS chip design consists mainly of Infomax filtering modules and scaling factor computation modules. In an Infomax filtering module, input samples are filtered by an Infomax filter with the weights updated by Infomax-driven stochastic learning rules. As for the scaling factor computation module, all operations including logistic sigmoid are integrated and implemented by the circuit design based on a piecewise-linear approximation scheme. The proposed architecture of this paper analysis the logic size and area using Xilinx.

Key Words- Convolutive Blind Source Separation (CBSS), Infomax, Scaling factor

1. INTRODUCTION

Blind source separation is a kind of a filtering process used to separate different sources from the mixed signals in which most of the information about sources and mixed signals is not known. This restriction makes the blind source separation a challenging task. Blind source separation becomes a very important research topic in a lot of fields such as audio signal processing, biomedical signal processing, communication systems and image processing. Simple version of mixing process is one in which without filtering effect instantaneous mixing occurs. Convolutive mixing process should be done for the audio source passing through a filtering environment before arriving at the microphones and in order to recover the original audio source

convoluted blind source separation should be done. One of the conventional methods is Independent component analysis (ICA) which is used to solve the CBSS problem. Major drawback of software implementation using this technique is often highly computational intensive and more time consuming process. Providing hardware solutions for ICA-based blind source separation has drawn considerable attention because of the hardware solution achieves optimal parallelism. An analog BSS chip can be designed using above-and-sub threshold CMOS circuit techniques which integrates an i/o interface of analog, weight coefficients and adoption blocks.

2. PROPOSED VLSI BLIND SOURCE SEPARATOR

The proposed CBSS system is shown in the FIG.2. The CBSS chip mainly consists of two functional cores: Infomax filtering module and scaling factor computation module. Additionally, the Infomax filtering outputs are added with the help of two small carry-save adders (CSAs). The current prototype chip is used for two sources and two sensors by utilizing four Infomax filtering modules along with two scaling factor computation modules.

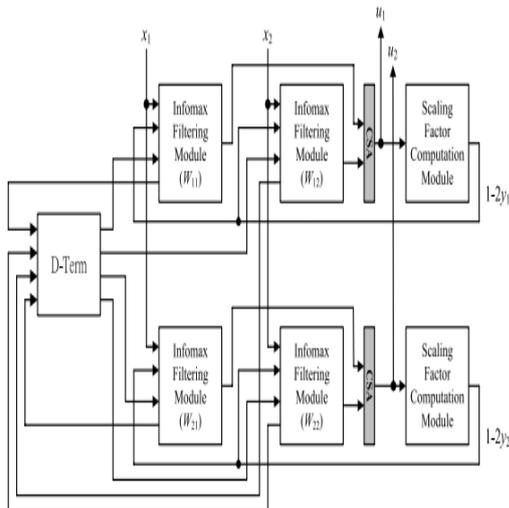


FIG 1: The block diagram of a proposed CBSS system

3. INFOMAX FILTERING MODULE

The Infomax filtering module for the proposed system is shown in fig.3. In the fig. 1, the CBSS separation network contains four causal FIR filters. These filters are adaptive because stochastic learning rules which are derived from the Infomax approach will alter the tap coefficients and are thus referred to herein as the Infomax adaptive filter or the Infomax filter. The Infomax filtering module is exemplified with six taps. In the Infomax filtering module, an input sample passes through lower and upper register

chains. These samples are multiplied with filter weights and scaling factors, respectively. The multiplication results of all of the taps are accumulated by a two-stage summation. The first stage adopts carry lookahead adders to generate the intermediate addition results for multiplication of every two successive taps. The above intermediate addition results are summed up by using a carry save addition scheme. A CSA(carry save adder) can accept more than two data inputs.

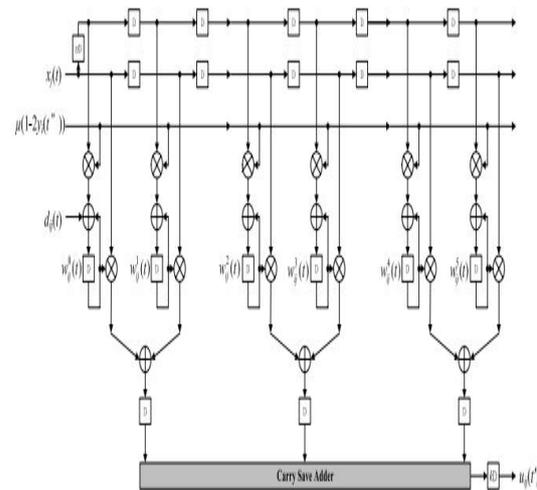


FIG 2: Infomax filtering module.

4. SCALING FACTOR COMPUTATION MODULE

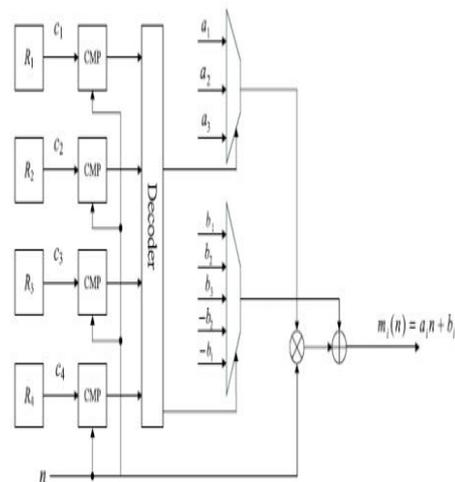


FIG 3: SCALING FACTOR COMPUTATION MODULE

Fig.3 describes the proposed circuit for the scaling factor computation module. The linear equation evaluation with input $u_i(t)$ and a_i and b_i are equation parameters and are implemented using a multiplier and an adder. In order to choose corresponding a_i and b_i , a line segment has to be selected by two multipliers. The scaling factor is calculated by using the formula $s(t) = 1 - 2y(t)$, where $y(t) = (1 + e^{-u(t)})^{-1}$. If $y(t)$ is known, $-2y(t)$ can be generated first using 2's complement and a left shift to $y(t)$. The scaling factor $s(t)$ is then obtained by adding $-2y(t)$ and one. The above procedure is simple. The scaling factor commutation is approximated directly rather than performing logistic sigmoid computation first and then calculating $1 - 2y(t)$. The target function to be approximated by linear piecewise scheme. To implement the line-segment approximation, the circuit design for scaling factor computation is to calculate single variable linear equations. For the equation of l_{si} which corresponding to $m_i(n) = a_i n + b_i$, $i = 1, 2, \dots, 5$, where $n = u_i(t)$. As the slopes of l_{s1} and l_{s5} are the same, these two line segments share the equation parameters a_1 . In the same manner, line segments l_{s2} and l_{s4} share the equation parameters a_2 . Furthermore, according to the symmetry in Fig. 5, the bias used for line segment l_{s5} , e.g., $-b_1$, is the negative of the bias b_1 used for line segment l_{s1} . In addition, line segments l_{s4} and l_{s2} use biases $-b_2$ and b_2 , respectively. As for the $d_{0ij}(t)$, this study designs a Dterm unit to execute $d_{ij}(t) = \text{cofactor}(w_{ij})(\det W_0)^{-1}$. The architecture of the D-term unit is shown in Fig. 6. The Dterm unit consists of a determinant circuit to find $\det W_0$ and in order to generate the inverse of $\det W_0$,

lookup table is used. Since W is a 2×2 matrix, the cofactors(w_{ij}) are w_{22} , $-w_{21}$, $-w_{12}$, and w_{11} , which are multiplied by $(\det W_0)^{-1}$ in parallel using four multipliers.

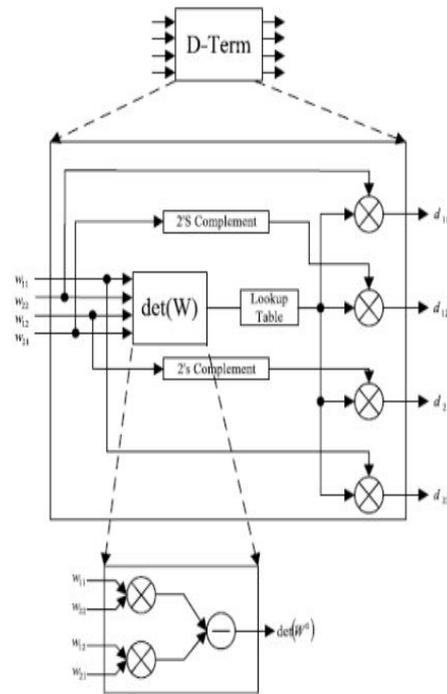


FIG 4: Architecture of a D-term unit

5. SIMULATION WAVEFORM

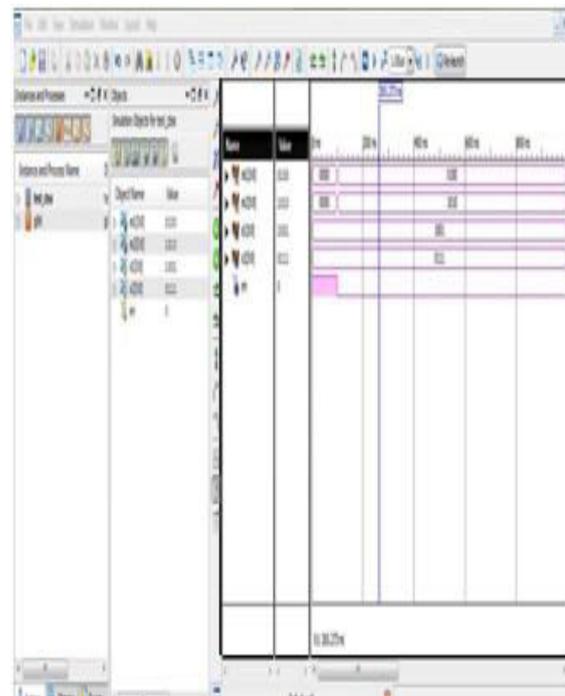


FIG 5: simulation result for the existing system

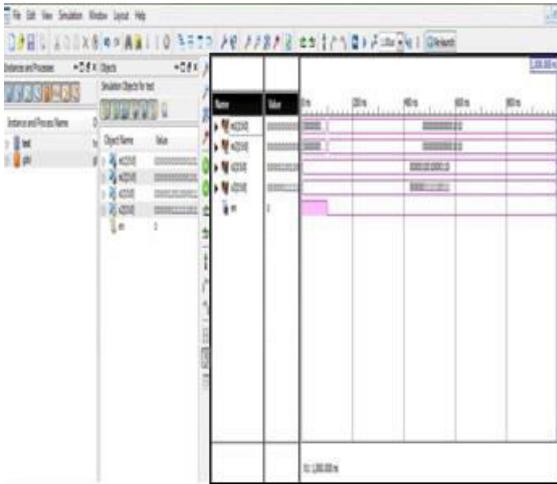


FIG 6: simulation result for the proposed CBSS 16bit

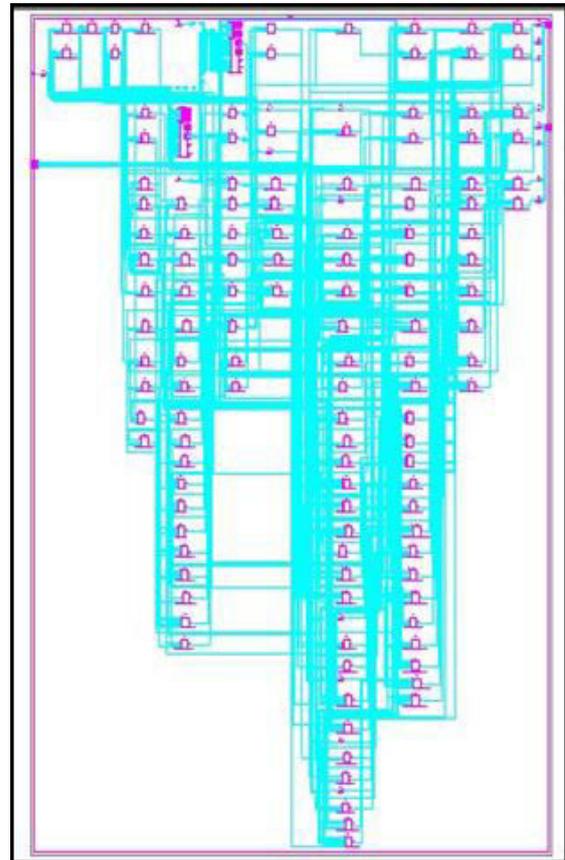


FIG 9: Technology schematic for the existing system

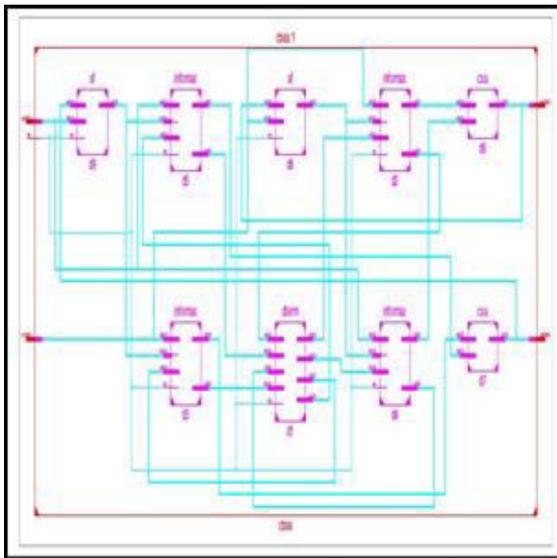


FIG 7: RTL for the existing system

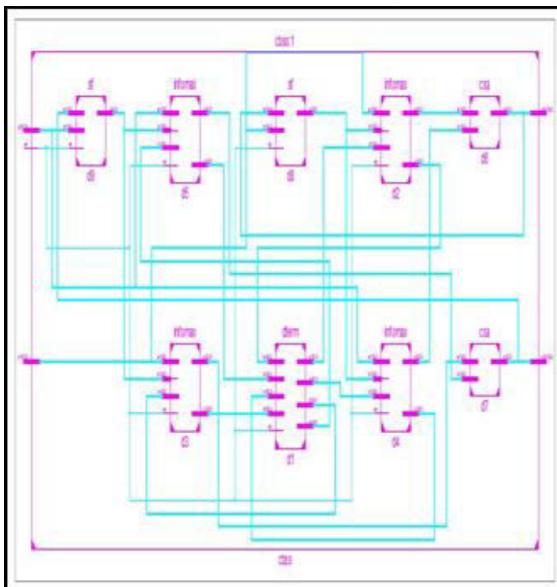


FIG 8: RTL for the proposed CBSS 16bit

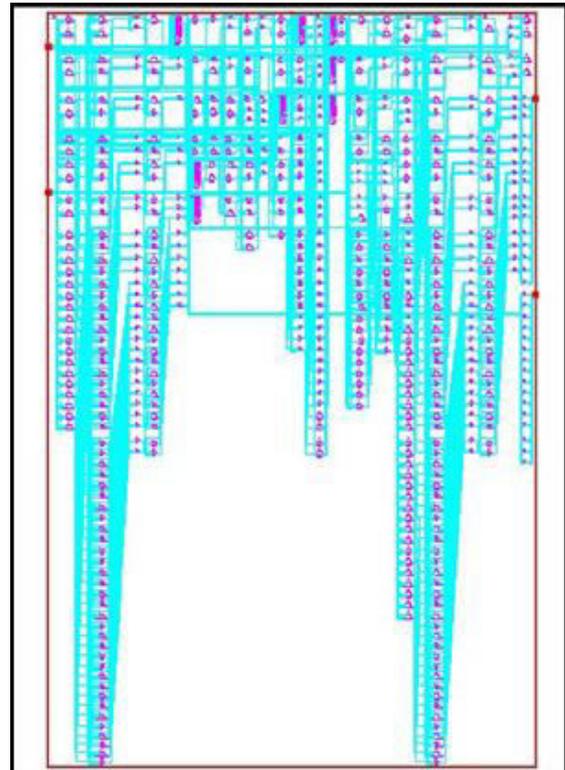


FIG 9: Technology schematic for the proposed CBSS 16bit

6. CONCLUSION

An efficient VLSI architecture design for CBSS with less delay has been presented in this paper. The architecture mainly consists of Infomax filtering modules and scaling factor computation modules and a D-term. CBSS separation network derived from the Infomax approach. The proposed system has high performance and has less delay as compared with the other existing system. By the usage of vedic multiplier in Infomax filter increases the speed as well as performance of the proposed system.

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