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LOW POWER THREE-INPUT XOR/XNOR WITH SYSTEMATIC CELL DESIGN METHODOLOGY

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Abstract: An efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style is proposed in this project. SCDM, which is an extension of CDM, plays the essential role in designing efficient circuits. At first, it is deliberately given priority to general design goals in a base structure of circuits. This structure is generated systematically by employing binary decision diagram. After that, concerning high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing. In the end, the resultant three-input XOR/XNORs enjoy fullswing and fairly balanced outputs.we can extend this project for designing of full adder design and it's topologies.

Index Terms: Binary decision diagram applications, energy efficiency, hybrid-CMOS logic style, systematic design methodology, three-input XOR/XNOR circuits.

I.INTRODUCTION:

The exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are the essential parts of several digital systems and are highly used in very large scale integration (VLSI)systems such as parity checkers, comparators, crypto processors, arithmetic and logic circuits, test pattern generators, especially in Full adder module as Sum output that is 3-input XOR and so forth. In most of these systems, XOR and XNOR gates constitute a part of the critical path of the system, which significantly affects the worst-case delay and the overall performance of the system. An optimized design is desired to avoid any degradation on the output voltage, consume less power, and have less delay in critical path with low supply voltage as we scale toward deep sub-micron technology. Other desired features for the design are to have a small number of transistors to implement the circuit. In particular, for XOR and XNOR circuits, the simultaneous generation of the two-non skewed outputs is highly desirable. As known, the switching speed of the balanced XOR and XNOR functions, comparing with those designs that use an inverter to generate the complement signal, is increased by eliminating the inverter from the critical path. Thus the design methodology for 3-input XOR/XNOR circuits is introduced.

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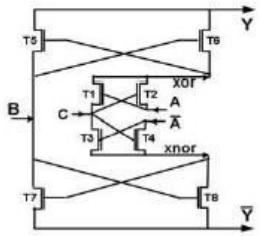
II. CELL DESIGN METHODOLOGY FOR LOWPOWER HIGH-SPEED BALANCED THREEINPUT XORXNOR IN HYBRID-CMOS LOGIC STYLE

The Introduction of Basic Cells This methodology is based on using different basic cells and optimization mechanisms. To obtain basic cells, 3-input XOR/XNOR function is investigated. For choosing the mechanisms, we use the simulation results of in which the balanced two inputs XOR/XNOR circuits based on the Cell2 have possessed better results.

A. Basic Cell: Version I:

We present the first version of the elementary basic cell (referred to as BC1) in "Fig. 1". In this cell, all six transistors are nMOS. Truth table of the BC1 in "Fig. 1" shows the output levels of this circuit for each input vector. To convert BC1 to an XOR–XNOR circuit that produces full swing output signals, it is necessary to replace high impedance outputs with logic "1" or "0". Moreover, in order to obtain better performance, non full-swing outputs for some input vectors must be converted into full swing signals.

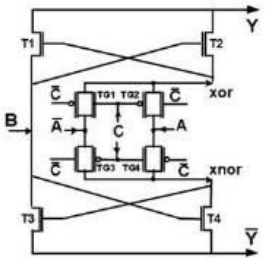


B	A	C	XOR3	XNOR3
0	0	0	Hi-z	Hi-z
0	0	1	Hi-z	0
0	1	0	Hi-z	Hi-z
0	1	1	0	Hi-z
1	0	0	Hi-z	0
1	0	1	0	1-
1	1	0	0	Hi-z
1	1	1	1-	0

Fig 1: BC1 circuit and input and output values

B. Basic Cell: Version II:

We present basic cell 2 (referred as BC2) in Fig. 2.3. In this cell, nMOS transistors for all four external section boxes and transition gate for central section boxes are selected. Fig. 2 shows outputs for each input vector. In order to convert the BC2 into an XOR–XNOR circuit, which provides full swing operation, it is necessary that the high impedance states of outputs in Fig. 2 be replaced with "1". We also have to optimize the circuit using various methods to eliminate the non full-swing operation.



B	A	C	XOR3	XNOR3
0	0	0	0	Hi-z
0	0	1	Hi-z	0
0	1	0	Hi-z	0
0	1	1	0	Hi-z
1	0	0	1-	0
1	0	1	0	1-
1	1	0	0	1-
1	1	1	1-	0

Fig 2: BC2 circuit and input and output values.

C. Correction and optimization mechanisms:

Correction and optimization mechanisms are pull up/down networks, feedback networks, bootstrap technique, output inverters and combinational mechanism named after applying the two mechanisms simultaneously on basic cell.

INTRODUCTION OF BALANCED 3-INPUT XOR-XNOR CIRCUITS

To convert these cells into balanced 3-input XORXNOR circuits with acceptable performance, two main steps should be employed. In the first step, the high impedance output states should be eliminated. In the second step, non fullswing output signals should be fixed. Three selected mechanisms such as feedback networks and combinational mechanisms such as pull up/down with feedback networks and pull up/down networks with

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bootstrap technique are applied and presented the circuits with names XO1 through XO6

INTRODUCTION OF XOR/XNOR CIRCUITS IN DIFFERENT CLASSES WITH THEIR MECHANISMS

A. Class A 3-input XOR-XNOR Circuits

A circuits are introduced (Table I). This group of circuits uses feedback network mechanisms to convert the basic cells into XOR-XNOR circuits providing full swing output signals. For each one of the basic cells, we select a proper feedback network. We present Class A circuits with the names XO1 and XO2 in Fig. 3.

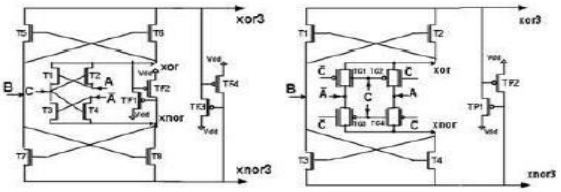

Fig 3: New 3-input XOR/XNOR Circuits-XO1 and XO2.

B. Class B 3-input XOR-XNOR Circuits

Class B circuits are a group of XOR-XNOR circuits (Table I) in which pull up and pull down networks and feedback networks are used simultaneously. In this class pull up and pull down networks are used to eliminate critical states and feedback networks are employed to rectify the output levels. Class B circuits, XO3 and XO4, are presented in Fig. 4.

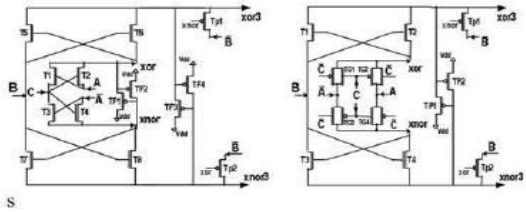

Fig 4: New 3-input XOR/XNOR Circuits-XO3 and XO4.

C. Class C 3-input XOR-XNOR Circuits

Class C circuits include XOR–XNOR circuits in which bootstrap technique has been used to ensure the full swing operation, and the high impedance states at the outputs have been corrected using pull up and pull down networks. This technique could be used for BC1 and BC2 since they all suffer from the no full voltage swing as well as the high impedance states at the output nodes. Circuits XO5 and XO6 in class C are optimized versions of BC1 and BC2 respectively. Class C circuits that are introduced in Table I and Fig.5 employ the combinational mechanisms.

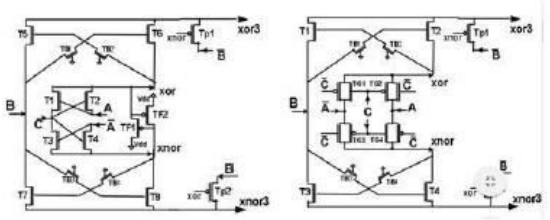

Fig 5: New 3-input XOR/XNOR Circuits-XO5 and XO6

III. SCDM FOR THREE-INPUT XOR/XNOR CIRCUITS INTRODUCTION

With the rapid growth of portable electronic devices, it is becoming a critical challenge to design low-power, high-speed (LPHS) circuits that occupy small chip areas. We see many published papers that compete in designing better circuits. Such studies mostly rely on creative design ideas but do not follow a systematic approach. As a consequence, most of them suffer from some different disadvantages.

1) They are implemented with logic styles that have an incomplete voltage swing in

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some internal nodes, which leads to static power dissipation.

2) Most of them suffer from severe output signal degradation and cannot sustain low-voltage operation.

3) They predominantly have dynamic power consumption for non-balanced propagation delay inside and outside circuits, which results in glitches at the outputs. Therefore, a well-organized design methodology can be regarded as a strong solution for the challenge. Cell design methodology (CDM) has been presented to design some limited functions, such as two-input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style.In the second stage, CDM is matured as systematic CDM (SCDM) in designing the three-input XOR/XNORs for the first time.

SCDM:

In this section, the methodology for threeinput XOR/XNORs is presented according to the flowchart. The design path is started by EBC systematic generation. In this step, general design goals are considered that the most distinctive ones are generating fairly balanced outputs, symmetric and powerground- free structure, fewer transistors in the critical path, as well as sharing common sub circuit. Systematic generation process of . In the remaining steps, the methodology offers opportunity to strive toward an assigned design target. Two of these steps include wisely selection of mechanisms and basic cells from PDP point of view. An indepth analysis for the selection Fig. in terms of PDP. In the last step, in order to put the resultant circuits in proper state, a sizing algorithm consistent with the methodology is indispensable.

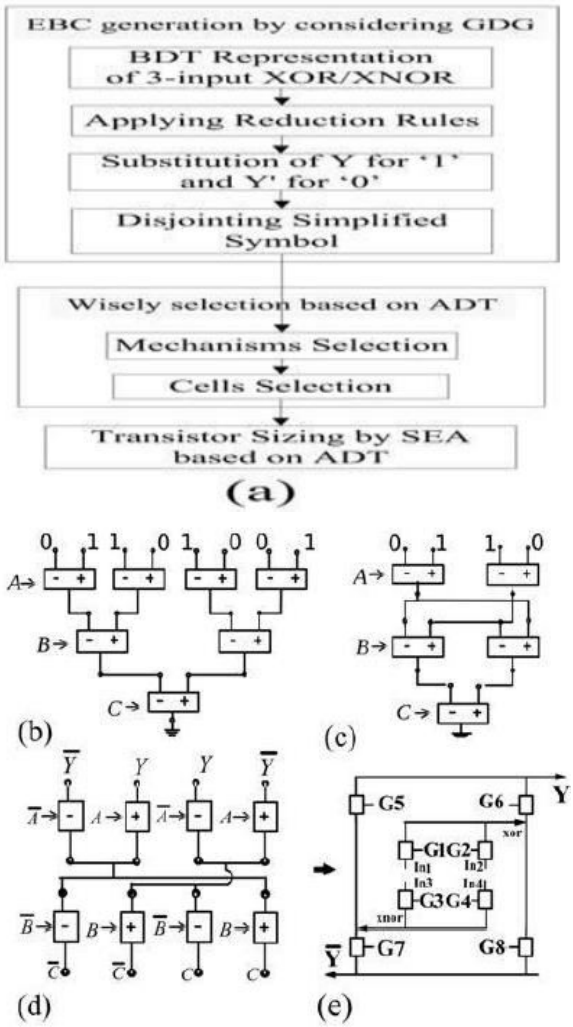

Fig. 6: (a) SCDM process for designing efficient three-input XOR/XNORs. (b) BDT representation of three-input XOR/XNOR function. (c) Applying reduction rules. (d) Substitution and disjointing. (e) EBC.

Elementary Basic Cell Systematic Generation

In order to generate the EBC of three-input XOR/XNOR circuits, four steps are taken. The process has been shown in Fig. 6(b)–

(e). Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) in order to share common sub circuits. The BDT is achieved by some cascaded 2 × 1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. This construction simply implements the minterms of the three-input XOR/XNOR function, as shown in Fig. 6(b). The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. The trees are acquired by impacting the state matrix on the corresponding control matrix where the multiply and add operators operate as follows:

The result of applying the reduction rules to the tree is shown in Fig. 6(c). Afterward, as the inputs into the first level are 0's and 1's of the function's truth table, the 0 and 1 can be replaced by the Y and Y, respectively. Finally, the simplified symbol can be divided into two distinct symbols:

1) the plus sign with the x input control and 2) the minus sign with the x input control. The result of applying steps 3 and 4 is shown in Fig. 6(d). The EBC, which is extracted from the above procedure, has been presented in Fig. 6(e). This cell has eight elements, deciding two outputs. We refer to the pins of the central section (IN1–IN4 and G1–G4) as A or C, or their complements. We also assume that pins of the external section G5– G8 can also be B or its complement. Wisely Selection of Mechanisms and Cells By replacing the elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is meditated to determine dominant mechanisms and cells, in terms of PDP, power, and delay when the optimization goal is PDP. The results are used to produce circuits for high performance portable electronic applications. Mechanisms include optimization mechanisms to resolve nonfull swing [inverter (I) and feedback (F)], correction mechanisms to resolve high impedance [pull up-down network (P) and feedback (F)], or the combinations of them [bootstrap-pull (BP) up-down, feedback pull (FP) up-down, bootstrap-feedback (BF), inverter-feedback (IF), and inverter-pull (IP) updown]. Mechanisms are divided into three categories:

1) cells with both nMOS and pMOS in EBC structure (C1);
2) onlynMOS (C2); and
3) onlypMOS (C3).

To reduce complexity, we have also considered the entral part of EBC and to achieve real results, the circuits have been simulated in the chain test bench. The circuits have been named with the abbreviation of the mechanism (or cell) being utilized, while the other circumstances, cells, or mechanisms are assumed to be fixed. Using transmission gates in EBC, which is called TG, the

complete circuit is achieved as there is no need for any other mechanisms. Therefore, TG is compared separately with others. The first experiment that studies the performance of the inverter mechanism shows I suffers from more power and PDP in comparison with other mechanisms. The increase in the static power consumption and switching delay of I are due to nonfull swing drive of the inverter. However, BP brings advantages in power reduction using blocking voltage in intermediate nodes to shift the gate voltage. The next experiment extends to investigate transistors' area of the mechanisms rather than the basic cells when the difference in circuits is their utilized mechanisms. We roughly estimated the transistors' area by adding the area (W × L) of all the transistors that is i Wi Li. Although the number of mechanism transistors in some cases is more than the basic cell transistors, BCTA occupies the most area in the majority of circuits. This is because the mechanism transistors are responsible for gate driving, such as in B, or resolving high impedance of only some states, such as in F and P, which are weaker responsibilities compared with that of the cell transistors for output generation. Therefore, the sizing algorithm also tends to choose the mechanism transistors' area to be smaller than BCTA.In the next experiment, we address feedback mechanism. The F network, when the cell is meditating to change the outputs, tries to keep the previous state, which gives rise to a struggle. This initial struggle causes the voltage step, as well as delay and power to increase. Therefore, the sizing algorithm chooses small sizes for F transistors not to be dominated. The struggle will be more critical when the F transistors are driven by the nonfull swing outputs or they should resolve solely the high impedance problem, because they should be strong enough to do the duty. The stronger the F transistors, the more the struggle and their consequences are more likely to happen. As a result, in these cases, it is better that high impedance duty is solved by P. The last experiment investigates the basic cells to characterize the cell, which outperforms in all mechanisms. According to the figure, C2 with the most numbers of nMOS transistors in its structure enjoys better results. The worst one is C3 with the largest number of pMOSs. Taken all the above points together, under the assumptions about the technology and the domain of circuits, the individual mechanism, I, does not present proper performance in terms of power and delay. This is while I was introduced as the only solution for nonfull swing outputs in many papers. Due to the high power consumption, I in combinational mechanism, such as IF and IP, operate worse than both BF and BP. The high impedance problem is also better resolved by P as we can observe IP to IF and BP to BF perform superior. Next, using transmission gate in EBC and TG enjoys the least power, delay, and PDP as a complete part that does not need any mechanisms. In the end, the individual mechanism, F, with suitable transistor sizing is capable of playing a key role besides the dominant combinational mechanisms, BP and FP, for the wisely design when PDP is target.Based on the findings, circuits with names XO1 through XO10 are presented, whose the

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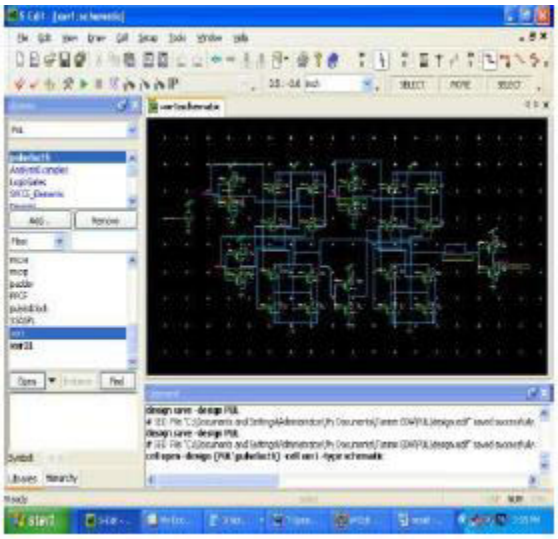
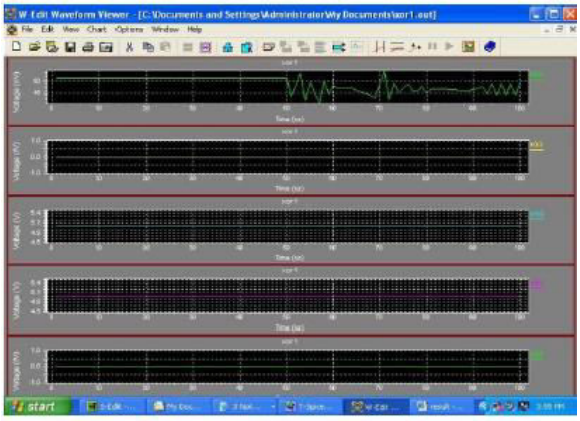
building structure details with the average PDP are tabulated in Table II

SCHEMATIC



WAVE FORM



COMPARISION TABLE

	EXISTING METHOD	PROPOSED METHOD
TRANSISTOR COUNT	26	22
POWER CONSUMED	3.96 mW	1.392 mW
DELAY	1.40 sec	0.89 sec
MAXIMUM POWER CONSUMED	5.529882e-005	2.598204e-005
MINIMUM POWER CONSUMED	3.926799e-009	1.392061e-009
AVERAGE POWER CONSUMED	8.678680e-007	1.451884e-007
TRANSIENT ANALYSIS	0.03 sec	0.01 sec

CONCLUSION:

SCDM serves as a design methodology for three-input XOR/XNOR, which is one of the most complex and competitive as well as all-purpose three-input basic gates in arithmetic circuits. This project has favored SCDM with the wise selection of the circuit components for the PDP target. In the end, three new high performance three-input XOR/XNOR circuits with less PDP and occupied area are conceived using SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay. The area utilization for the proposed circuits enjoys improvement with the advantages of regularity and symmetry in layout.

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