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A NOVEL CONTROL METHOD FOR TRANSFORMERLESS HBRIDGE CASCADED STATCOM WITH STAR CONFIGURATION

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Abstract- This paper imposes a multilevel H-bridge converter with star configuration based on Transformerless static synchronous compensator (STATCOM) system. This proposed control methods devote themselves not only to the current loop control but also to the dc capacitor voltage control. The passivity-based controller (PBC) theory is used in this cascaded structure STATCOM for the first time. By adopting a proportional resonant controller an overall voltage control is realized same as the DC capacitor voltage control and an active disturbance rejection controller will provide clustered balancing control. In a field programmable gate array, individual balancing control is achieved by vertically shifting modulation wave. 10KV, 2MVA rated two actual H-bridge cascaded STATCOMs are constructed and a series of verification are executed in simulink MATLAB simulations. Two actual H-bridge cascaded STATCOMs rated at 10 kV 2 MVA are constructed and a series of verification tests are executed. The dc capacitor voltage can be maintained at the given value effectively with fuzzy logic controller .

Index Terms— Active disturbances rejection controller (ADRC), H-bridge cascaded, passivitybased control (PBC), proportional resonant (PR) controller, Fuzzy logic controller, shifting modulation wave, static synchronous compensator (STATCOM).

I INTRODUCTION

Flexible ac transmission systems (FACTS) are being increasingly used in power system to enhance the system utilization, power transfer capacity as well as the power quality of ac system interconnections [1], [2]. As a typical shunt FACTS device, static synchronous compensator (STATCOM) is utilized at the point of common connection (PCC) to absorb or inject the required reactive power, through which the voltage quality of PCC is improved [3]. In recent years, many topologies have been applied to the STATCOM. Among these different types of topology, H-bridge cascaded STATCOM has been widely accepted in high-power applications for the following advantages: quick response speed, small volume, high efficiency, minimal interaction with the supply grid and its individual phase control ability [4]–[7]. Compared with a diode-clamped converter or flying capacitor converter, H-bridge cascaded STATCOM can obtain a high number of levels more easily and can be connected to the grid directly without the bulky transformer. This enables us to reduce cost and improve performance of H-bridge cascaded STATCOM [8].There are two technical challenges which exist in H-bridge cascaded STATCOM to date. First, the control method for the current loop is an important factor influencing the compensation performance. However, many nonideal factors, such as the limited bandwidth of the output current loop, the time delay induced by the signal detecting circuit, and the reference command current generation process, will deteriorate the compensation effect. Second, H-bridge cascaded STATCOM is a complicated system with many H-bridge cells in each phase, so the dc capacitor voltage imbalance issue which caused by different active power losses among the cells, different switching patterns for different cells, parameter variations of active and passive components inside cells will influence the reliability of the system and even lead to the collapse of the system. Hence, lots of researches have focused on seeking the solutions to these problems. In terms of current loop control, the majority of approaches involve the traditional linear control method, in which the nonlinear equations of the STATCOM model are linearized with a specific equilibrium. The most widely used linear control schemes are PI controllers [9], [10]. In [9], to regulate reactive power, only a simple PI controller is carried out. In [10], through a decoupled control strategy, the PI controller is employed in a synchronous d–q frame. However, it is hard to find the suitable parameters for designing the PI controller and the performance of the PI controller might degrade with the external disturbance. Thus, a number of intelligent methods have been proposed to adapt the PI controller gains such as particle swarm optimization [11], neural networks [12], and artificial immunity [13]. In literature [14], [15], adaptive control and linear robust control have been reported for their anti-external disturbance ability. In literature [16], [17], a popular dead-beat current controller is used. This control method has the high bandwidth and the fast reference current tracking speed. The steady-state performance of H-bridge cascaded STATCOM is improved, but the dynamic performance is not improved. To enhance robustness and simplify the controller design, a passivity-based controller (PBC) based on error dynamics is proposed for STATCO [27]–[30]. Furthermore, the exponential stability of system equilibrium point is guaranteed. Nevertheless, these methods are not designed on the basis of STATCOM with the H-bridge cascaded structure and there are no experimental verifications in these literatures.. In this paper, a new nonlinear control method based on PBC theory which can guarantee Lyapunov function dynamic stability is proposed to control the current loop. It performs satisfactorily to improve the steady and dynamic response. For dc capacitor voltage balancing control, by designing a proportional resonant (PR) controller for overall voltage control, the control effect is improved, compared with the traditional PI controller. Active disturbances rejection controller (ADRC) is first proposed by Han in his pioneer work [49], and widely employed in many engineering practices [50]–[53]; furthermore, it finds its new application in H-bridge cascaded STATCOM for clustered balancing control. It realizes the excellent dynamic compensation for the outside disturbance. By shifting the modulation wave vertically for individual balancing control, it is much easier to be realized in field-programmable gate array (FPGA) compared with existing methods. Two actual H-bridge cascaded STATCOMs rated at 10 kV 2 MVA are constructed and a series of verification tests are executed. The experimental results have verified the viability and effectiveness of the proposed control methods.

II. CONFIGURATION OF THE 10KV 2MVA STATCOM SYSTEM

Fig. 1 shows the circuit configuration of the 10 kV 2 MVA star-configured STATCOM cascading 12 H-bridge pulse width modulation (PWM) converters in each phase and it can be expanded easily according to the requirement. By controlling the current of STATCOM directly, it can absorb or provide the required reactive current to achieve the purpose of dynamic reactive current compensation. Finally, the power quality of the grid is improved and the grid offers the active current only. The power frequency of 1 kHz. Then, with a cascade number of N=12, the ac voltage cascaded results in a 25-level waveform in line to neutral and a 49-level waveform in line to line. In each cluster, 12 carrier signals with the same frequency as 1 kHz are phase shifted by 2π/12 from each other. When a carrier frequency is as low as 1 kHz, using the method of phase-shifted uni-polar sinusoidal PWM, it can make an equivalent carrier frequency as high as 24 kHz. The lower carrier frequency can also reduce the switching losses to each cell. As shown in Fig. 2, the main digital control block diagram of the 10 kV 2 MVA STATCOM experimental system consists of a digital signal processor (DSP) (Texas Instruments TMS320F28335), an FPGA (Altera CycloneIII EP3C25), and 36 complex programmable logic devices (CPLDs) (Altera MAXII EPM570). Most of the calculations, such as the detection of reactive current and the computation of reference voltage, are achieved by DSP. Then, DSP sends the reference voltages to the FPGA. The FPGA implements the modulation strategy and generates 36 PWM switching signals for each cell. CPLD of each cell receives PWM switching signal from the FPGA and drives IGBTs.

III. CONTROLALGORITHM

algorithm for H-bridge cascaded STATCOM. The whole control algorithm mainly consists of four parts, namely, PBC, overall voltage control, clustered balancing control, and individual balancing control. The first three parts are achieved in DSP, while the

last part is achieved in the FPGA

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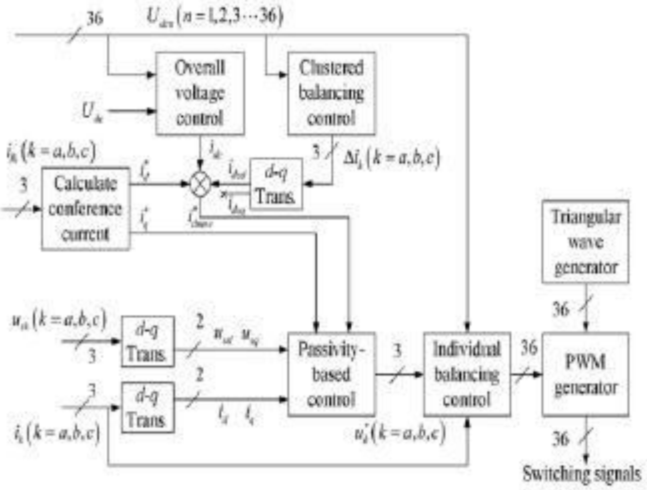
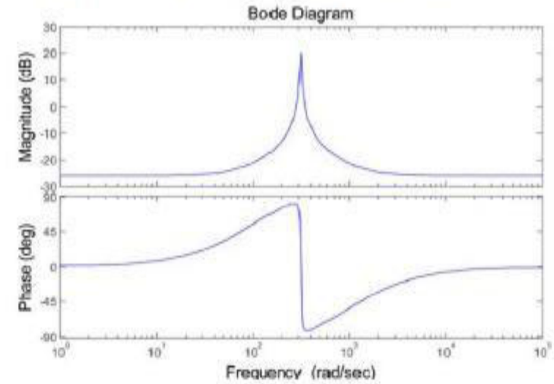


OVERALL VOLTAGE CONTROL

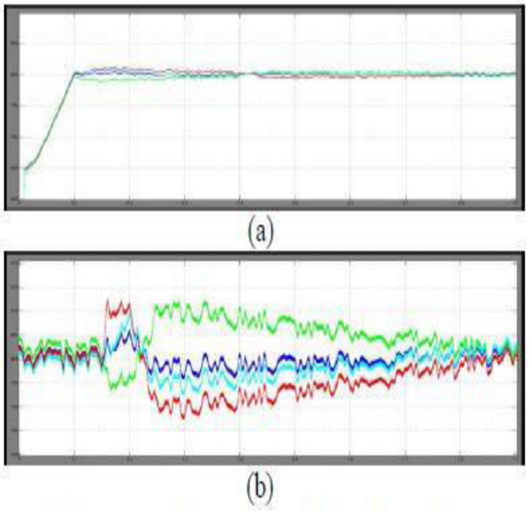
As the first-level control of the dc capacitor voltage balancing, the aim of the overall voltage control is to keep the dc mean voltage of all converter cells equalling to the dc capacitor reference voltage. The common approach is to adopt the conventionalPI controller which is simple to implement. However, the output voltage and current of H-bridge cascaded STATCOM are the power frequency sinusoidal variables and the output power is the double power frequency sinusoidal variable, it will make the dc capacitor also has the double power frequency ripple voltage. By setting the cutoff frequency and the resonant frequency of the PR controller appropriately, it can reduce the part of ripple voltage in total error, decrease the reference current distortion which is caused by ripple voltage, and improve the quality of STATCOM output current.The PR controller is composed of a proportional regulator and a resonant regulator. influences the gain of the controller but the bandwidth.

This paper selects k□ =0.05, k□=10,ω□ =3.14rad/s, and ω□ = 100π as the controller parameters. Fig. 5 shows the bode plots of the PR controller with the previous parameters and Fig. 6 shows the block diagram of overall voltage control. The signal of voltage error is obtained by comparing the dc mean voltage of all converter cells with the dc capacitor reference voltage. Then, the signal of voltage error is regulated by the PR controller and delivered to the current loop as a part of the reference current. U□□ is the dc capacitor reference voltage. is the mean value of overall voltage. is the active control current for overall voltage control.



SIMULATION RESULTS

To verify the correctness and effectiveness of the proposed methods, the experimental platform is built according to the second part of this paper. Two Hbridge cascaded STATCOMs are running simultaneously.


(a)

(b)

CONCLUSION

This paper has analyzed the fundamentals of STATCOM based on multilevel H-bridge converter with star configuration. And then, the actual H-bridge cascaded STATCOM rated at 10 kV 2 MVA is constructed and the novel control methods are also proposed in detail with fuzzy logic. The proposed methods has the following characteristics.A PBC theory-based nonlinear controller is first used in STATCOM with this cascaded structure for the current loop control, and the viability is verified by the experimental results with fuzzy