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Title: A Novel approach of 4*4 Vedic Multiplier using Reversible Logic Gates.

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A Novel approach of 4*4 Vedic Multiplier using Reversible Logic Gates

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ABSTRACT-

The performance of the multiplier determines the system performance, because the multiplier is slowest element in the system. Multiplication is one of the major operation in arithmetic and logical operations and multiplier is used in many applications like FFT, DFT, Image enhancement, DWT etc,. The multiplication speed influences the processor speed, so the speed of the multiplication should be high. There is one such promising solution i.e., Vedic multiplier. Vedic multiplier is designed using Vedic mathematics. Vedic mathematics is an ancient system of mathematics, which is formulated by Sri Jagadguru Bharathi Krishna tirthaji (1884-1960). The word Vedic is obtained from the word Veda‖ which gives the meaning of power house of knowledge and devine. This paper proposes the novel approach of 4*4 Vedic multiplier using reversible logic gates. Design of high speed Vedic multiplier is designed based on Vedic mathematics Vedic mathematic. Usage of reversible logic gates leads to reduction of power dissipation. Power dissipation is an important factor which can‘t be neglected in VLSI. The multiplier is designed using ―Urdhva Tiryakbhyam‖ sutra from Vedic mathematics which is different from conventional multiplier like array and booth multiplier. The coding is done using VHDL for 2*2 Vedic multiplier and simulation is done using Xilinx 14.5 tool. The logic verification of the modules has been done by usingModelsim.

Keywords: Vedic mathematics, Vedic multiplier, Urdhva Tiryakbhyam, Reversible logic gates, garbage outputs, constant inputs, quantum cost, gate counts.

I. INTRODUCTION

Multiplier has many applications like FFT, DFT and image enhancement. In order to increase the operation speed of FFT, DFT the multiplication process should be faster. Compared to basic multiplier like Wallace and array multiplier Vedic multiplier is faster and it consumes less power. The entire speed and the performance of the system is depends on the speed of the addition and multiplication taking place in the system. Delay will be more due to the long multiplication process, and the propagation delay will also be considered because of the parallel adders used in the addition stage.The multiplication done in threeways: Partial Products Generation (PPG), Partial Products Addition (PPA) and Final Convectional Addition. The main issue is to increase the speed of the multiplier partialproducts should be reduce. Vedic mathematics is an ancient system of mathematics, which formulated by Sri Jagadguru Bharathi Krishna tirthaji (1884-1960). The word Vedic is obtained from the word ―Veda‖ which gives the meaning of power house of knowledge and devine. These are 16 sutras in Vedic mathematics Urdhva Tiryakbhyam and Nikhilam Navatascaramam Dasatah are traditionally taken to design multiplier. Vedic multiplier does not produce any partial products so the number of adders required in the multiplier is less which leads to simplicity of the circuit. There are 16 sutras in

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Vedic mathematics and 13 upa sutras (sub formulae). Out of 16 sutras Urdhva Tiryakbhyam sutra is used to design the Vedic multiplier.

1.1 Reversible logic:

Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modelled using reversible logic. In 1961 Mr. R. Landauer showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of KT*ln2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Then in 1973 Mr.C.H. Benett showed that this heat dissipation due to information loss can be avoided if the circuitis designed using reversible logic gates [2]. A gate is considered to be reversible only iffor each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n –input, n- output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit. While designing the circuit using reversible logic gates the designer should concentrate on the following parameters: 1. Garbage Outputs (GO): Indicates the unused outputs in the circuit which cannot be avoided and it is necessary to achieve reversibility. The circuit should contain minimum number of garbage outputs. 2. Constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

3. Gate Counts (GC): Indicates the number of reversible gates that are required to design the circuit, so that the circuit should contain reversible gates as minimum as possible.
4. Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. Some of the reversible logic gates are shown below that are used in the proposed design:

PERES GATE:

It is a 3*3 reversible gate i.e., it has three inputs and three outputs. The representation of Peres gate is shown below. Quantum cost of this gate is 4.

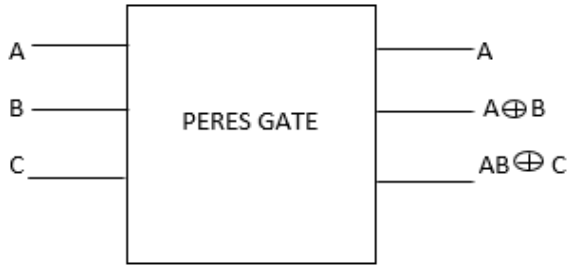

Fig.1: Peres gate.

Peres gate is one of the popular gate and used in many applications.

TOFFOLI GATE:

It is a 3*3 reversible gate i.e., it has three inputs and three outputs. The representation of Toffile gate is shown below. Quantum cost of this gate is 5.

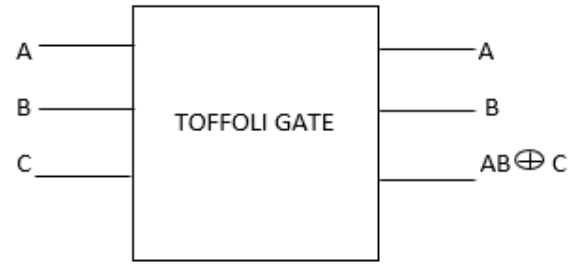

Fig.2: Toffoli gate.

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BME GATE:

It is a 4*4 reversible gate i.e., it has four inputs and four outputs. The representation of BME gate is shown below. The quantum cost of this gate is 6.

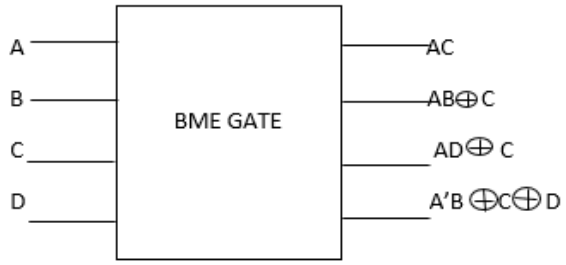

Fig.3: BME gate.

II. URDHVA TIRYAKBHYAM MULTIPLICATION ALGORITHM

The Sanskrit word Urdhva Tiryakbhyam which gives a meaning of vertical and crosswise in English. Vedic mathematics and design using Urdhva Tiryakbhyam sutra. This sutra can be apply to Binary, Hex and Decimal multiplication and it generates all partial products concurrently. Fig. shows the 4*4 Binary multiplication using Urdhva Tiryakbhyam sutra and can also be used for N*N bit multiplication. This multiplier does not depend on the processor clock frequency, because both partial products and sums are calculated concurrently. The net advantage is that it eliminates the requirement of microprocessor to operate at increasingly higher clock frequencies. As the number of switching instances increases the operating frequency of a processor also increases. It leads to higher power consumption and also heat dissipation results in increased device operating temperature. The scalability T is the one more advantage of Vedic multiplier which is designed using Urdhva Tiryakbhyam sutra. As the input and output data bus widths increases the processing power also increases because of its regular structure. Due to its regular structure it can be easily layout in a silicon chip and consumes less area. If the number of input bits increases the gate delay increases drastically in conventional multiplier but it is slow in Vedic multiplier. Therefore the Vedic multiplier designed using Urdhva Tiryakbhyam sutra is efficient in terms of time, space and power. The below figure explains the algorithm. Multiplication of 101 by 110.

1. First need to take right hand digits from both multiplicand and multiplier. Then multiply them together. Then we will get the LSB digit of the answer.
2. Multiply second bit of the top number with the LSB of the bottom number. Then multiply LSB of the top number with the second bit of the bottom number. Then add them together to get second bit of the answer.
3. Multiply third bit of the bottom with the LSB of the top number, second bit of the bottom number with the second bit of the top number, LSB of the bottom number with the third bit of the top number. Then add them together to get third bit of the answer.
4. This step is same as second step, just move one place to the left. We will multiply the second digit of one number by the MSB of the other number.
5. Finally multiply the LSB of the top and bottom number to get final product.

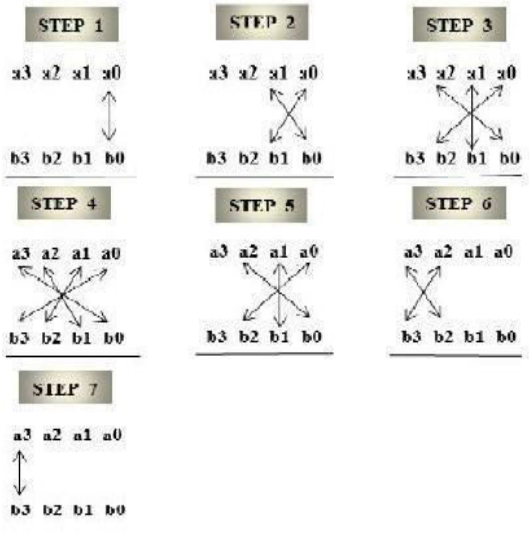

fig.4: multiplication of two 4 bit numbers using urdhvatiryakbhyam

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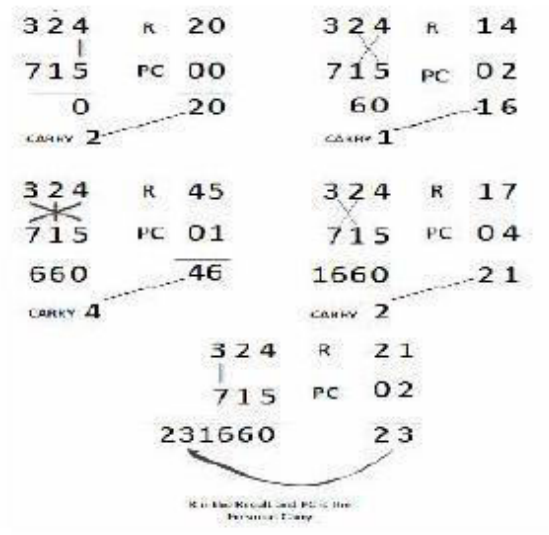

fig.5: urdhvatiryakbhyam algorithm for decimal multiplication.

III. PROPOSED WORK

The hardware realization of 2*2 multiplier which is designed using conventional gates is shown in fig. the expression for the outputs i.e., q0, q1, q2, q3are shown in fig. The 2*2 multiplier which is designed using reversible gates based on Vedic mathematics is shown in fig. the circuit requires a total of 5 reversible logic gates out of five, 3 gates are Peres gates and remaining gates are Toffile gate and BME gate. The quantum cost of 2*2 Urdhva Tiryakbhyam multiplier is enumerated to be 23. The number of garbage outputs are 7. The number of constant inputs are 5. The 4*4 reversible Vedic multiplier is designed using 2*2 Vedic multiplier. The block diagram of 4*4 Vedic multiplier is shown in fig. The block diagram consists of four 2*2 multiplier blocks each block has four bits as inputs. Two bits from the multiplicand and another two bits from multiplier. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder are obtained from the second 2*2 multiplier. The output of the second and third 2*2 Vedic multiplier block is given to the 4-bit ripple carry adder as an input which is designed using reversible HNG gate. The output of second ripple carry adder is given to the first 4-bit ripple carry adder. The sum 2-bits from first four bit ripple carry adder is taken as output of the 4*4 Vedic multiplier. Another 2-bits sum output is given as an input to the third 4-bit ripple carry adder. The 4- bit output is taken from the fourth 2*2 Vedic multiplier and given as an input to the third 4-bit ripple carry adder. The output of this block indicates the output of last four bits of the 4*4 Vedic multiplier. In this design the ripple carry adder is designed using HNG gate. The quantum cost of this design is 166. The number of gates used in this design is 32. The number of constant inputs used in this design is 32. The garbage outputs in this design is 60.

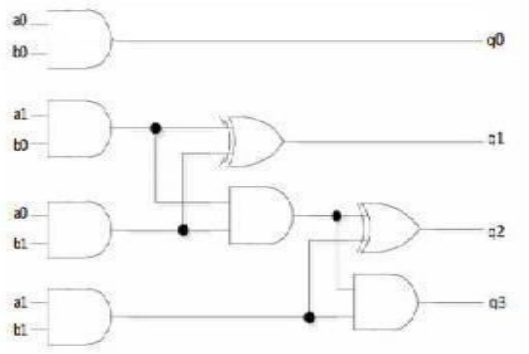

Fig. 6:2*2 Vedic multiplier using conventional gates.

q0= a0.b0
q1= (a1.b0) xor (a0.b1)
q2= (a0.a1.b0.b1) xor (a1.b1)
q3= a0.a1.b1.b0

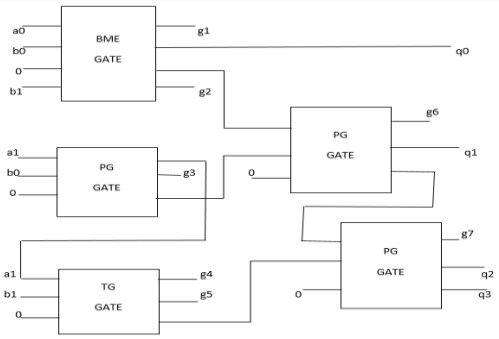

Fig.7: proposed 2*2 Vedic multiplier using Reversible logic gates.

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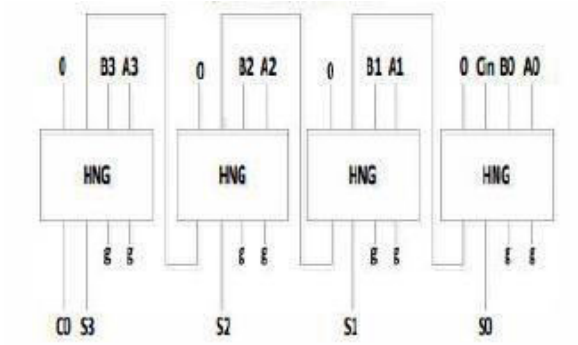

4-bit Ripple Carry Adder units

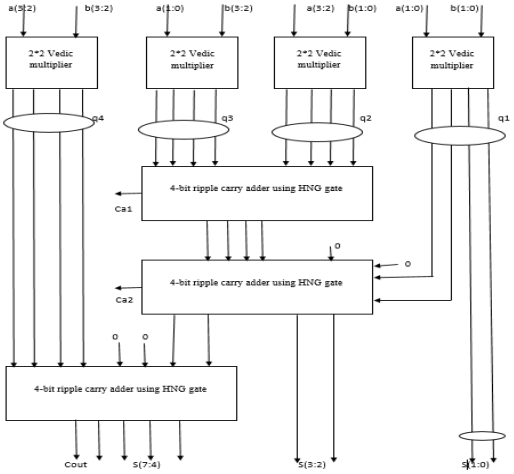

Fig.9: Block diagram of Reversible 4*4 Vedic multiplier.

IV. RESULT ANALYSIS AND COMPARISION

The 2*2 and 4*4 reversible Vedic multiplier is designed and logically verified using XILINX 14.4 and Modelsim. The proposed 2*2 and 4*4 Vedic multiplier is implemented using VHDL coding.

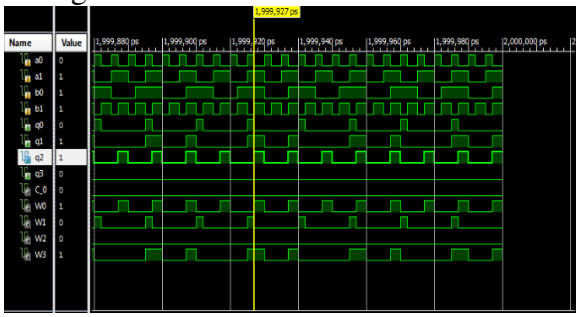

Fig.10: Simulation results for reversible 2*2 Vedic multiplier.

Fig.11: Simulation results for reversible 4*4 Vedic multiplier.

	Garbage output	Constant inputs	Gate counts	Quantum cost
Existing system 2*2	9	4	6	21
Existing system 4*4	62	29	37	162
Proposed method 2*2	7	5	5	23
Proposed method 4*4	60	32	32	166

Table.1: comparison of proposed method with the existing system.

V. CONCLUSION

The proposed architecture of reversible Vedic multiplier exhibits speed improvements. The multiplier designed using Urdhva Tiryakbhyam sutra is efficient compared to existing system.

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