International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

ENHANCED CARRY INCREMENT ADDER USING HAN-CARLSON & KOGGE-STONE ADDER TECHNIQUES

[1]K.SAMBASIVA RAO, [2]M.BALA RAMA KRISHNA, [3]G.NARESH, [4]L.SAI SRUTHIK GOUD, [5]M.YESHWANTH REDDY

[1]*Assistant Professor, ECE, TEEGALA KRISHNA REDDY ENGINEERING COLLEGE*
[2345]*UG. SCHOLAR, ECE, TEEGALA KRISHNA REDDY ENGINEERING COLLEGE*

ABSTRACT

This project focuses on the design and performance enhancement of a Carry Increment Adder (CIA) through a two-stage approach, aiming to optimize key metrics such as speed, power consumption, and area in arithmetic circuit design. In **Stage 1**, the CIA is implemented using a **Kogge-Stone Adder (KSA)**, which employs a parallel prefix architecture. This design offers significantly higher speed compared to traditional Ripple Carry Adder (RCA)-based CIAs by minimizing propagation delay. The KSA-based CIA is particularly well-suited for high-speed computational applications where performance is critical. In **Stage 2**, the project progresses to developing a CIA based on the **Han-Carlson Adder (HCA)**. The HCA utilizes a hybrid parallel prefix structure that combines elements of both Kogge-Stone and Brent-Kung adders, resulting in improved power efficiency and reduced area usage. This stage is designed to optimize the adder for low-power, area-constrained environments, making it ideal for compact and energy-efficient VLSI systems.

By systematically transitioning from a high speed KSA based design to a more power and area efficient HCA based implementation, the project showcases clear advancements in adder architecture. These developments offer valuable insights into the creation of high-performance, efficient arithmetic units suitable for modern VLSI applications.

I.INTRODUCTION

The design of efficient arithmetic circuits is a cornerstone of modern digital systems, particularly in high-performance applications such as processors, digital signal processors (DSPs), and application-specific integrated circuits (ASICs). Among the various arithmetic operations, binary addition is fundamental, and its efficiency directly impacts the overall system performance. Traditional adder architectures, such as the Ripple Carry Adder (RCA), have limitations in speed due to their sequential carry propagation. To address these limitations, advanced adder structures like the Kogge-Stone Adder (KSA) and Han-Carlson Adder (HCA) have been developed, offering significant improvements in speed, power consumption, and area efficiency.

International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

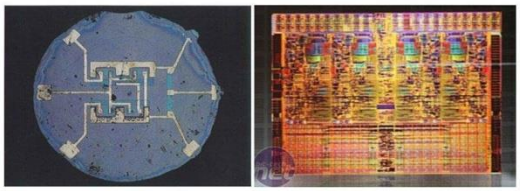

Fig1: A comparison :first planar IC(1961) and Intel Nehalem quad core die.

The Carry Increment Adder (CIA) is a specialized adder designed to handle the carry increment operation efficiently, which is crucial in applications like binary counters and certain cryptographic algorithms. The performance of the CIA can be significantly enhanced by integrating advanced adder techniques. This project explores the enhancement of the CIA through the incorporation of the Kogge-Stone and Han-Carlson adder techniques, aiming to achieve superior performance metrics in terms of speed, power, and area.

The Kogge-Stone Adder, introduced by Kogge and Stone in 1973, utilizes a parallel prefix structure to compute carries in logarithmic time, making it one of the fastest adder architectures. On the other hand, the Han-Carlson Adder, a hybrid of the Kogge-Stone and Brent-Kung adders, offers a balance between speed and area efficiency, making it suitable for low-power and compact applications. By integrating these advanced adder techniques into the CIA, this project aims to leverage their strengths to enhance the overall performance of the adder.

In the subsequent sections, we will delve into the literature surrounding these adder techniques, examine existing configurations of the CIA, propose an enhanced configuration incorporating the Kogge-Stone and Han-Carlson adder techniques, and conclude with the anticipated benefits and potential applications of the enhanced CIA.

II. LITERATURE REVIEW

The evolution of adder architectures has been driven by the need for faster and more efficient arithmetic operations in digital systems. Early adder designs, such as the Ripple Carry Adder, while simple, suffered from significant delays due to the sequential propagation of carry bits. To mitigate this, Carry Lookahead Adders (CLAs) were introduced, which compute carries in parallel, reducing propagation delay.

The Kogge-Stone Adder (KSA) is a type of CLA that employs a parallel prefix structure to compute carries in logarithmic time. This approach significantly reduces the critical path delay, making the KSA one of the fastest adder architectures. The KSA operates by recursively combining generate and propagate signals from pairs of bits, allowing for the computation of carries in parallel. This parallelism leads to a substantial reduction in carry propagation delay, which is critical in high-speed applications.

However, the KSA's high speed comes at the cost of increased area and power consumption due to the extensive wiring

required for the parallel prefix structure. To address these issues, various optimizations have been proposed, including the use of sparse Kogge-Stone adders, which reduce the number of carry signals generated, thereby decreasing area and power consumption.

The Han-Carlson Adder (HCA) is another advanced adder architecture that combines elements of the Kogge-Stone and Brent-Kung adders. The HCA utilizes a hybrid parallel prefix structure that balances the speed of the KSA with the area efficiency of the Brent-Kung adder. This balance makes the HCA suitable for applications where both speed and area efficiency are critical. The HCA operates by combining generate and propagate signals in a manner that reduces the number of stages required for carry computation, leading to a reduction in area and power consumption compared to the KSA.

In the context of the Carry Increment Adder (CIA), integrating these advanced adder techniques can lead to significant improvements in performance. The CIA, which is designed to handle the carry increment operation efficiently, can benefit from the reduced carry propagation delay offered by the KSA and the area and power efficiency of the HCA. Previous studies have demonstrated the advantages of incorporating advanced adder techniques into the CIA, leading to enhanced performance metrics.

III. EXISTING CONFIGURATION

The traditional configuration of the Carry Increment Adder (CIA) utilizes the Ripple Carry Adder (RCA) as its core component. The RCA, while simple and easy to implement, suffers from significant delays due to the sequential propagation of carry bits. In the context of the CIA, this delay becomes a bottleneck, limiting the overall performance of the adder.

To address this limitation, various enhancements have been proposed, including the use of Carry Lookahead Adders (CLAs) to compute carries in parallel. While CLAs reduce carry propagation delay, they still require substantial area and power resources. The Kogge-Stone Adder (KSA), with its parallel prefix structure, offers a significant improvement in speed but at the cost of increased area and power consumption.

The Han-Carlson Adder (HCA) provides a balance between speed and area efficiency, making it a suitable candidate for enhancing the CIA. By integrating the HCA into the CIA, it is possible to achieve improved performance metrics without a significant increase in area and power consumption.

3.1: BLOCK DIAGRAM OF HALF ADDER

International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

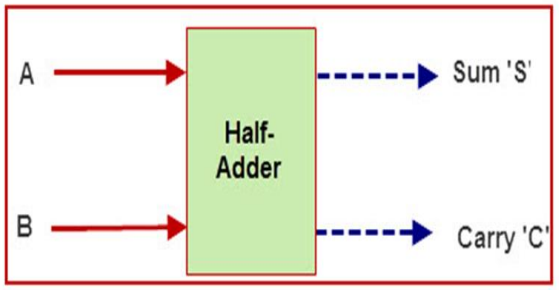

Fig 3.1: Block diagram of half adder

Truth Table of Half Adder:

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3.2 :BLOCK DIAGRAM OF FULLADDER

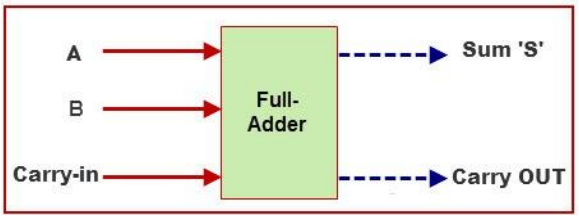

Fig 3.2: Block diagram of full adder

TRUTH TABLE OF FULL ADDER:

INPUTS			OUTPUT	
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

IV. PROPOSED CONFIGURATION

The proposed configuration of the Carry Increment Adder (CIA) integrates the Kogge-Stone Adder (KSA) and the Han-Carlson Adder (HCA) techniques to enhance performance in terms of speed, power, and area. The integration of these advanced adder architectures into the CIA aims to leverage their strengths to achieve superior performance metrics.

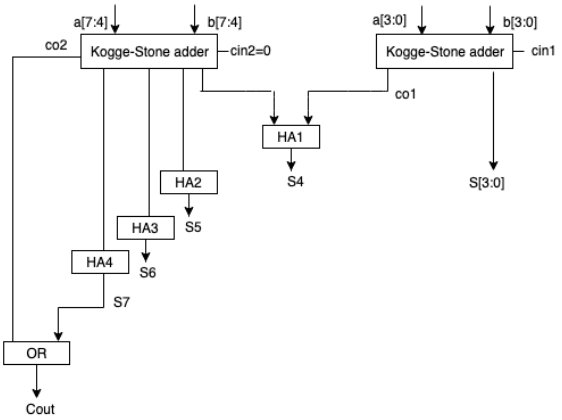

Fig 4.1: Block diagram of CIA using KOGGE-STONE(8-bit)

In the proposed configuration, the KSA is utilized to compute carries in parallel, significantly reducing carry propagation delay and enhancing speed. The HCA is employed to balance the speed of the KSA

International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

with area and power efficiency, ensuring that the enhanced CIA remains suitable for low-power and compact applications.

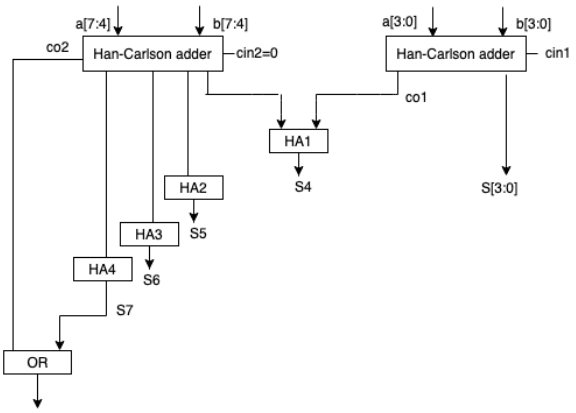

Fig 4.2: Block diagram of CIA using HAN-CARLSON(8-bit)

The integration of the KSA and HCA into the CIA involves modifying the carry

computation logic to incorporate the parallel prefix structures of the KSA and HCA. This modification allows for the efficient computation of carries, leading to improved performance metrics.

V. RESULT

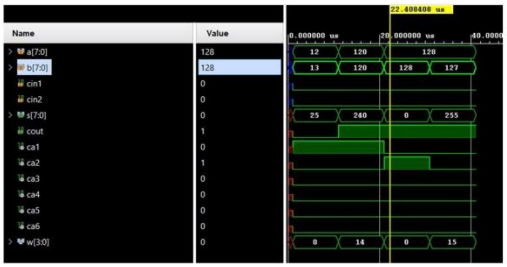

Fig5.1: Simulation of CIA_RCA, CIA_HCA, CIA_KSA.

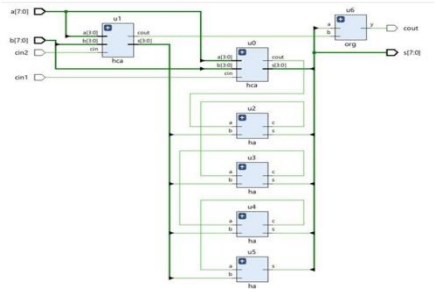

Fig 5.2: RTL schematic of CIA_HCA.

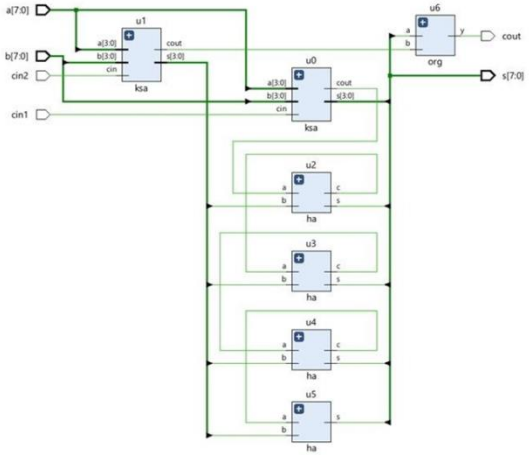

Fig 5.3: RTL schematic of CIA_KSA.

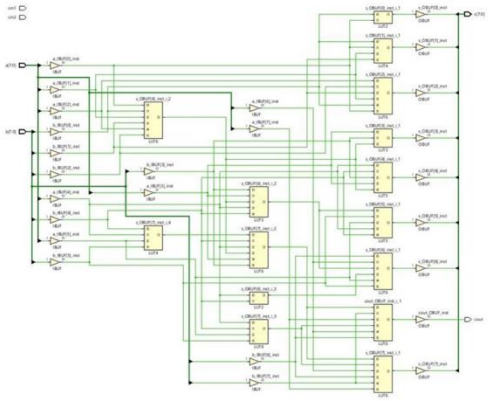

Fig 5.4: Technology schematic of CIA_HCA.

International Journal for Innovative Engineering and Management Research
PEER REVIEWED OPEN ACCESS INTERNATIONAL JOURNAL
www.ijiemr.org

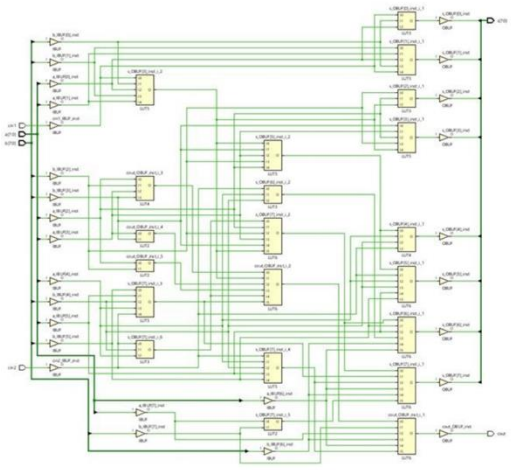

Fig 5.5: Technology schematic of CIA_KSA.

Fig 5.6: Power consumption of CIA_RCA.

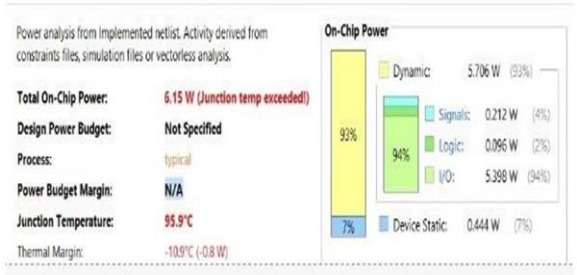

Fig 5.7: Power consumption of CIA_KSA.

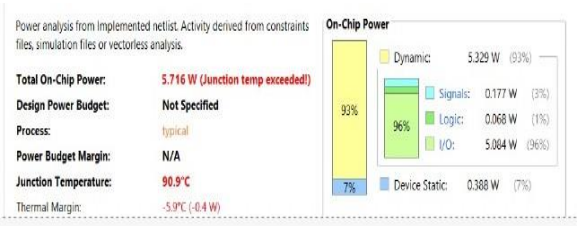

Fig 5.8: Power consumption of CIA_HCA.

	Area	Power
CIA_RC	27 IOB 13 Slice LUT	6.393W
CIA_KS	27 IOB 16 Slice LUT	6.15W
CIA_HCA	25 IOB 11 Slice LUT	5.716W

Fig 5.9: Comparison of power consumption & area utilization of CIA_RCA, CIA_KSA, CIA_HCA.

CONCLUSION

The integration of the Kogge-Stone and Han-Carlson adder techniques into the Carry Increment Adder (CIA) represents a significant advancement in adder architecture design. By leveraging the parallel prefix structures of the KSA and HCA, it is possible to achieve enhanced performance in terms of speed, power, and area.

The proposed configuration of the CIA offers a balanced approach, combining the high-speed capabilities of the KSA with the area and power efficiency of the HCA. This balance makes the enhanced CIA suitable

for a wide range of applications, from high-performance processors to low-power embedded systems.

Future work in this area could explore further optimizations, such as the use of sparse Kogge-Stone adders to reduce area and power consumption, and the integration of other advanced adder techniques to further enhance performance. Additionally, the application of the enhanced CIA in various digital systems could provide valuable insights into its practical performance and potential areas for improvement.

REFERENCES

1. Kogge, P. M., & Stone, H. S. (1973). A parallel algorithm for the efficient solution of a general class of recurrence equations. *IEEE Transactions on Computers*, C-22(8), 786–793.
2. Han, C. S., & Carlson, D. A. (1987). Fast area-efficient VLSI adders. *IEEE Transactions on Computers*, C-36(1), 40–44.
3. Sklansky, J. (1960). Conditional-sum addition logic. *IRE Transactions on Electronic Computers*, EC-9(2), 226–231.
4. Knowles, S. (2001). A family of adders. *Element 14*.
5. Beaumont-Smith, A., & Lim, C. C. (2001). Parallel prefix adder design. *IEEE*.
6. Shirriff, K. (2025). Reverse-engineering a carry-lookahead adder in the Pentium. *January 2025*.
7. Mun'im Zabidi, M., & Abdullah, M. (2020). Architecture of 8-bit Kogge-Stone Adder. *Applied Physics Express*.
8. ElProCus. (2023). Kogge-Stone Adder: Circuit, Working, and Applications. Retrieved from https://www.elprocus.com/kogge-stone-adder/
9. Wikipedia contributors. (2025). Kogge–Stone adder. In *Wikipedia, The Free Encyclopedia*. Retrieved from https://en.wikipedia.org/wiki/Kogge%E2%80%93Stone_adder
10. Azhagu Jaisudhan Pazhani, A. (2022). Computation unit architecture for satellite image processing systems. *Earth Science Informatics*.
11. GeeksforGeeks. (2021). 4 Bit Binary Incrementer. Retrieved from https://www.geeksforgeeks.org/4-bit-binary-incrementer/
12. SlideServe. (2023). CMOS VLSI Design Lecture 11 Adders. Retrieved from https://www.slideserve.com/Thomas/introduction-to-cmos-vlsi-design-lecture-11-adders
13. SpringerLink. (2022). Quaternary Carry Increment Adder. *Wireless Personal Communications*.
14. Wikipedia contributors. (2025). Han–Carlson adder. In *Wikipedia, The Free Encyclopedia*. Retrieved from https://en.wikipedia.org/wiki/Han%E2%80%93Carlson_adder
15. Zabidi, M. M., & Abdullah, M. (2020). Architecture of 8-bit Kogge-Stone Adder. *Applied Physics Express*.
16. ElProCus. (2023). Kogge-Stone Adder: Circuit, Working, and Applications.

Retrieved from https://www.elprocus.com/kogge-stone-adder/

17. Wikipedia contributors. (2025). Kogge–Stone adder. In *Wikipedia, The Free Encyclopedia*. Retrieved from https://en.wikipedia.org/wiki/Kogge%E2%80%93Stone_adder
18. Azhagu Jaisudhan Pazhani, A. (2022). Computation unit architecture for satellite image processing systems. *Earth Science Informatics*.
19. GeeksforGeeks. (2021). 4 Bit Binary Incrementer. Retrieved from https://www.geeksforgeeks.org/4-bit-binary-incrementer/
20. SlideServe. (2023). CMOS VLSI Design Lecture 11 Adders. Retrieved from https://www.slideserve.com/Thomas/introduction-to-cmos-vlsi-design-lecture-11-adders